What is claimed is:

1. A method of decoding an image encoded in a digital camcorder format comprising:

a preprocessing step of detecting a position of an end of block (EOB) of respective discrete cosine transform (DCT) blocks using length information of a variable-length code of an encoded bit stream of the image; and

a step of redefining a processing order of the DCT blocks according to the position of the EOB detected at the preprocessing step, and performing a variable-length decoding with respect to the respective DCT blocks in the redefined processing order.

2. The method as claimed in claim 1, wherein when a video segment is composed of M macro blocks, a macro block is composed of N DCT blocks, and respective basic areas are allocated to the macro block and the DCT block, respectively;

the DCT block whose EOB is produced within the basic area of the DCT block is called a 'complete DCT block', and the contrary DCT block is called an 'incomplete DCT block';

the macro block where all the EOBs of N DCT blocks are produced within the basic area of the macro block is called a 'complete macro block', and the contrary macro block is called an 'incomplete macro block';

DCT block index vectors are used for separating and rearranging the complete DCT blocks and the incomplete DCT blocks; and

Macro block index vectors are used for separating and rearranging the complete macro blocks and the incomplete macro blocks.

3. The method as claimed in claim 2, wherein the variable-length decoding step performs the variable-length decoding in the order of the complete DCT block in the complete macro block, the incomplete DCT block in the complete macro block, the complete DCT block in the incomplete macro block, and the incomplete DCT block in the incomplete macro block in the corresponding video segment in accordance with contents of the DCT block index vectors and the macro block index vectors.

4. The method as claimed in claim 2, wherein M DCT block index vectors are used for the macro blocks, the number of elements in the respective vector is the same as the number of the DCT blocks in the macro block, and the respective element includes a complete DCT block (CDB) counter, an EOB counter, a DCT address register 0, a DCT address register 1, and a DCT address register 2;

wherein the DCT address register 0 stores the number of the first complete DCT block having a surplus bit stream, and is used for initializing the DCT address register 1;

wherein the DCT address register 1 and the DCT address register 2 store values indicating the elements of the DCT block index vector; and

wherein the CDB counter and the EOB counter count the number of complete DCT blocks and the number of EOBs in the macro block, respectively.

5. The method as claimed in claim 2, wherein the number of elements in the macro block index vector is the same as the number of the macro blocks in the video segment, and the element includes a macro block (MB) address register 1, an MB address register 2, and a complete macro block (CMB) counter;

wherein the MB address register 1 and the MB address register 2 store values indicating elements of the macro block index vector; and

wherein the CMB counter counts the number of complete macro blocks in the video segment.

6. The method as claimed in claim 1, wherein a bit address register is used for storing a bit address where the variable-length decoding is stopped, and is allocated to each DCT block;

wherein the bit address register stores a position where the variable-length decoding is stopped (i.e., a position where the decoding is resumed at a next decoding process) in case of an incomplete DCT block; and

wherein in case that an end of block (EOB) is detected from the corresponding DCT block, the bit address register stores a next bit address (i.e., a start position of a surplus bit stream).

7. The method as claimed in claim 2, wherein the preprocessing step comprises the steps of:

initializing values of a DCT address register 1, a DCT address register 2, a complete DCT block (CDB) counter, and an EOB counter of all DCT block index vectors, and values of a macro block (MB) address register 1, an MB address register 2, and a complete macro block (CMB) counter of macro block index vector;

if the DCT block is the complete DCT block, writing a position of a bit following the EOB in a bit address register, writing the corresponding DCT block number in an element indicated by the address register in the DCT block index vector, increasing values of the address register, the CDB counter, and the EOB counter, and if the DCT block is the incomplete DCT block, resuming the process of the incomplete DCT block after reinitializing the values of the DCT address register 1 and the DCT address register 2;

if the DCT block is the incomplete block, writing a position where the decoding is stopped in the bit address register, writing the DCT block number in a position indicated by the address register 2 in the DCT block index vector, decreasing the value of the address register 2, resuming the decoding in a

position indicated by the bit address register in the incomplete DCT block, and reading out a bit that exceeds the basic area subsequently from a position indicated by the bit address register of the complete DCT block; and

sequentially performing the above steps with respect to the N DCT blocks in the macro block.

8. The method as claimed in claim 7, wherein the step of resuming the process of the incomplete DCT block stores an address of the vector element having the number of the incomplete DCT block to be processed in the DCT address register 2, stores an address of the vector element having the number of the completed DCT block from which the bit stream to be used for decoding the incomplete DCT block is to be read out in the DCT address register 1, reads out the bit position in which the decoding of the incomplete DCT block is to be resumed from the bit address register of the incomplete DCT block, and reads out the position in which the bit stream is to be read out from the complete DCT block from the bit address register of the complete DCT block.

9. The method as claimed in claim 7, wherein the step of resuming the process of the incomplete DCT block comprises the steps of:

if the EOB is detected from the incomplete DCT block, increasing the value of the EOB counter, and judging whether the value is smaller than N;

if it is judged that the increased value of the EOB counter is smaller than N, decreasing the value of the address register 2, selecting a new incomplete DCT block with reference to the element indicated by the value of the address register 2, and then continuing the decoding of the selected incomplete DCT block; and

if it is judged that the increased value of the EOB counter is N, writing the number of the present macro block is written in the element indicated by the MB address register 1, and increasing the value of the MB address register 1 and the value of the CMB counter.

10. The method as claimed in claim 7, wherein the step of resuming the process of the incomplete DCT block comprises the steps of:

if the surplus bit stream of the basic area allocated to the complete DCT block vanishes completely, increasing the value of the DCT address register 1, and judging whether the value is smaller than the value of the CDB counter;

if it is judged that the increased value of the DCT address register 1 is smaller than the value of the CDB counter, selecting a new complete DCT block with reference to the element

indicated by the value of the DCT address register 1, and continuing the decoding using the surplus bit stream of the basic area allocated to the selected complete DCT block; and

if it is judged that the increased value of the DCT address register 1 is the same as the value of the CDB counter, writing the number of the present macro block in the element indicated by the MB address register 2, and decreasing the value of the MB address register 2.

11. The method as claimed in claim 2, wherein the variable-length decoding step preferentially variable-length-decodes the complete DCT block stored in a DCT address register 1 of a DCT block index vector that corresponds to the complete macro block stored in a macro block (MB) address register 1 of a macro block index vector.

12. The method as claimed in claim 2, wherein the variable-length decoding step completes the process of a complete macor block, and comprises the steps of:

(a) initializing a DCT address register 0, an address register 1, an address register 2, and an EOB counter of all the DCT block index vectors, and an address register 1 and an address register 2 of the macro block index vectors;

(b) if a completed DCT block is processed, increasing the value of the EOB counter and the value of the address register 1 of the DCT block index vector, and processing a new complete DCT

block determined by the increased value of the DCT address register 1;

(c) repeating the step (b) until the value of the DCT address register 1 coincides with the value of the CDB counter.

(d) after performing the step (c), initializing the value of the DCT address register 1, and processing the incomplete DCT block by the value of the DCT address register 2 in a manner that the bit stream is read out with reference to the value of the bit address register of the incomplete DCT block to be processed, and if the bit stream of the basic area vanishes completely, the bit stream is subsequently read out from a corresponding position with reference to a bit address register of the complete DCT block selected by the DCT address register 1;

(e) if the bit stream of the basic area allocated to the complete DCT block vanishes completely, increasing the values of the DCT address register 0 and the DCT address register 1, and selecting a next complete DCT block by a value of a new DCT address register 1;

(f) if an incomplete DCT block is processed, increasing the value of the EOB counter, decreasing the value of the DCT address register 2, and processing a new incomplete DCT block determined by the DCT address register; and

(g) performing the above steps (d)~(f) are performed until the value of the EOB counter becomes N, and then storing a

position of a next bit where a final EOB is found in the bit address register of the present complete DCT block.

13. The method as claimed in claim 12, wherein the variable-length decoding step further comprises the steps of:

(h) if the process of a complete macro block is completed through the step (g), increasing the value of the MB address register 1 of the macro block index vector, and if the increased value is smaller than the value of the CMB counter, processing the complete macro block corresponding to the number of the macro block of the element indicated by the value of the MB address register 1;

(i) repeating the above steps (b)~(h) until the value of the MB address register 1 of the macro block index vector coincides with the value of the CMB counter;

(j) if the step (i) is performed, initializing values of the MB address register 1 of the macro block index vector and the address register 1 of all the DCT block index vectors;

(k) processing the incomplete macro block that corresponds to the number of the macro block of the element indicated by the value of the MB address register 2; and

(l) repeating the step (k) until the value of the MB address register 1 of the macro block index vector coincides with the value of the CMB counter.

14. The method as claimed in claim 13, wherein the step (k) includes the steps of:

preferentially processing the complete DCT blocks by sequentially performing the steps (b) and (c), and then processing the incomplete DCT blocks by sequentially performing the steps (d)~(f);

if the value of the address register 1 of the DCT block index vector is the same as the value of the CDB counter, increasing the value of the MB address register 1 of the macro block index vector, and if the increased value is smaller than the value of the CMB counter, selecting a new complete macro block, and then selecting a new complete DCT block with reference to the value of the address register 1 of the DCT block index vector allocated to the new complete macro block to continue the decoding; and

if the value of the EOB counter is N, decreasing the value of the MB address register 2 of the macro block index vector, and selecting and processing a next incomplete according to the decreased value.

15. An apparatus for decoding an image encoded in a digital camcorder format comprising:

a preprocessor for detecting a position of an end of block (EOB) of respective discrete cosine transform (DCT) blocks using

length information of a variable-length code of an encoded bit stream of the image;

a variable-length decoding section for redefining a processing order of the DCT blocks according to a position of the EOB detected by the preprocessor, and performing a variable-length decoding with respect to the respective DCT blocks in the redefined processing order;

a storage device for receiving and outputting to the preprocessor the encoded bit stream, and storing and outputting the EOB of the respective DCT block outputted from the preprocessor and DCT coefficients variable-length-decoded by the variable-length decoding section; and

a control section having built-in DCT block index vectors, macro block index vectors, and a bit address register to redefine a variable-length decoding order of the variable-length decoding section, and outputting to the storage device the number of the respective DCT blocks to be processed, a read signal, and a write signal in accordance with values of the DCT block index vectors.

16. The apparatus as claimed in claim 15, wherein when a video segment is composed of M macro blocks, a macro block is composed of N DCT blocks, and respective basic areas are allocated to the macro block and the DCT block, respectively, the DCT block whose EOB is produced within the basic area of the DCT block is called a 'complete DCT block', and the contrary DCT

block is called an 'incomplete DCT block', the macro block where all the EOBs of N DCT blocks are produced within the basic area of the macro block is called a 'complete macro block', and the contrary macro block is called an 'incomplete macro block';

the variable-length decoding section performs the variable-length decoding in the order of the complete DCT block in the complete macro block, the incomplete DCT block in the complete macro block, the complete DCT block in the incomplete macro block, and the incomplete DCT block in the incomplete macro block in the corresponding video segment in accordance with contents of the DCT block index vectors and the macro block index vectors.

17. The apparatus as claimed in claim 15, wherein the preprocessor prepares a simple code table according to a length stored in a variable-length code table of the variable-length decoding section, and performs a pseudo-variable-length decoding accordingly.

18. The apparatus as claimed in claim 15, wherein M DCT block index vectors of the control section are used for the macro blocks in order to separate and rearrange the complete DCT blocks and the incomplete DCT blocks, the number of elements in the respective vector is the same as the number of the DCT blocks in the macro block, and the respective element includes a complete DCT block (CDB) counter, an EOB counter, a DCT address register 0, a DCT address register 1, and a DCT address register 2;

wherein the DCT address register 0 stores the number of the first complete DCT block having a surplus bit stream, and is used for initializing the DCT address register 1;

wherein the DCT address register 1 and the DCT address register 2 store values indicating the elements of the DCT block index vector; and

wherein the CDB counter and the EOB counter count the number of complete DCT blocks and the number of EOBs in the macro block, respectively.

19. The apparatus as claimed in claim 15, wherein the macro block index vectors of the control section are used for separating and rearranging the complete macro blocks and the incomplete macro blocks, the number of elements in the macro block index vector is the same as the number of the macro blocks in the video segment, and the element includes a macro block (MB) address register 1, an MB address register 2, and a complete macro block (CMB) counter;

wherein the MB address register 1 and the MB address register 2 store values indicating elements of the macro block index vector; and

wherein the CMB counter counts the number of complete macro blocks in the video segment.

20. The apparatus as claimed in claim 15, wherein a bit address register of the control section is used for storing a bit

address where the variable-length decoding is stopped, and is allocated to each DCT block;

wherein the bit address register stores a position where the variable-length decoding is stopped (i.e., a position where the decoding is resumed at a next decoding process) in case of the incomplete DCT block; and

wherein in case that an end of block (EOB) is detected from the corresponding DCT block, the bit address register stores a next bit address (i.e., a start position of a surplus bit stream).